Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1	("6026017").PN.	US-PGPUB; USPAT	OR	OFF	2005/05/24 14:37
L2	1	("5867425").PN.	US-PGPUB; USPAT	OR	OFF	2005/05/24 15:36
L3	12187	(control adj gate) and (floating adj gate)	US-PGPUB; USPAT	OR	ON	2005/05/24 16:42
L4	11480	3 and drain	US-PGPUB; USPAT	OR	ON	2005/05/24 16:42
L5	1841	4 and (source with pair)	US-PGPUB; USPAT	OR	ON	2005/05/24 15:54
L6	1209	5 and (dope or doping or implant or implanting or implantation)	US-PGPUB; USPAT	OR	ON	2005/05/24 16:42
L7	690	6 and @ad<"20010731"	US-PGPUB; USPAT	OR	ON	2005/05/24 15:39
L8	310	7 and ((floating adj gates) with pair)	US-PGPUB; USPAT	OR	ON	2005/05/24 16:42
L9	7555	(control adj gate) and (floating adj gate)	USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/05/24 16:42
L10	4056	9 and drain	USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/05/24 16:42
L11	697	10 and (dope or doping or implant or implanting or implantation)	USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/05/24 16:42
L12	26	11 and ((floating adj gates) with pair)	USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/05/24 16:43

US-PAT-NO: 6088263

DOCUMENT-IDENTIFIER: US 6088263 A
See image for Certificate of Correction

TITLE: Non-volatile memory using substrate electrons

---------- KWIC ---------

Abstract Text - ABTX (1):

A nonvolatile memory cell which is highly scalable includes a cell formed in a triple well. A **pair of sources for a pair** of cells on adjacent word lines each acts as the emitter of a lateral bipolar transistor. The lateral bipolar transistor of one cell operates as a charge injector for the other cell. The charge injector provides carriers for substrate hot carrier injection onto a **floating gate**.

Brief Summary Text - BSTX (3):

Nonvolatile memory cells are advantageous since they retain recorded information even when the power to the memory is turned off. There are several different types of nonvolatile memories including erasable programmable read only memories (EPROMs), electrically erasable and programmable read only memories (EEPROMs) and flash EEPROM memories. EPROMS are erasable through light exposure but are electrically programmable by channel hot electron injection onto a **floating gate**. Conventional EEPROMs have the same programming functionality, but instead of being light erasable they can be erased and programmed by electron tunneling facilitated by an on-chip electrical signal. Thus, information may be stored in these memories, retained when the power is off, and the memories may be erased for reprogramming, as necessary, using appropriate techniques. Flash EEPROMs may be block erased, typically giving them better read access times than regular EEPROMs.

Brief Summary Text - BSTX (6):

Nonvolatile memory cells differ in certain respects from the transistors that are generally utilized in electronic components called logic devices, such as microcontrollers, that work with the memory cells. Logic devices are formed of transistors that use a single gate electrode. Nonvolatile memories usually include two gate electrodes, known as the control and **floating gate** electrodes, situated one adjacent to the other. Because of this structural difference, nonvolatile memories and logic devices may be made by different processes.

This may contribute to a substantial increase in process complexity and manufacturing cost when the two components need to be placed together into the same chip.

Brief Summary Text - BSTX (7):

Particularly with an EEPROM, the electrical programming of the cells normally requires substantial potentials to be applied to the cells. These potentials induce electron tunneling from an N+ region onto the **floating gate**. Additional complexity may arise from the need to provide substantially larger voltages to memory cells than are needed for normal logic transistor operation.

Brief Summary Text - BSTX (9):

Furthermore, with the conventional flash EEPROMs, the electrical programming of the cells normally requires high current to be applied to the cells. A very minute fraction of this electron current becomes injected from the **drain** depletion region onto the **floating gate**. This means that the injection efficiency of such devices is low (e.g., 1.times.10.sup.-6 to 1.times.10.sup.-9). The requirement of high current adds additional complexity because of the design of the high current pump operated at low voltage.

Brief Summary Text - BSTX (11):

In accordance with one embodiment, a memory array including word lines and bit lines includes a first and second cell, each having a **control gate, floating gate** and a source formed in a substrate. The **control gate** is situated over the **floating gate**. The cells are each adapted to form a depletion region in the substrate. A **drain** is situated between the first and second cells, each of the cells being part of a different word line.

Drawing Description Text - DRTX (7):

FIG. 6 is a greatly enlarged cross-sectional view of the **drain implant**;

Drawing Description Text - DRTX (8):

FIG. 7 is a greatly enlarged cross-sectional view of the source **implant**; and

Drawing Description Text - DRTX (9):

FIG. 8 is a greatly enlarged cross-sectional view of the logic device implanted by the source **implant**.

Detailed Description Text - DETX (2):

Referring to the drawing wherein like reference characters are used for like parts throughout the several views, a pair of memory cells 10a and 10b, shown in FIG. 1, are located in two adjacent word lines 12a and 12b. The cells 10

are both arranged on the same bit line 14. Other cells 16, 18, and 20 are arranged on bit lines 22, 24, and 26 and word lines 12. This structure is advantageously implemented on a semiconductor layer having situated thereon electrically isolated **floating gates** 28.

Detailed Description Text - DETX (3):
The source terminal 30 of each cell 10, 16, 18 and 20 is controlled by a source 32 or 34. The **control gates** 36a and 36b of the cells 10, 16, 18 and 20 are controlled by the word lines 12. The **drains** 38 of the cells are connected to the bit lines 14, 22, 24 and 26.

Detailed Description Text - DETX (4):
One layout for implementing a pair of cells 10, shown in FIG. 3, includes a pair of **control gates** 36a and 36b. The same layout may be used for the other pairs of cells 16, 18 and 20. The **control gates** 36 extend across a field oxide isolation region 40 which is bordered by the **drain** 38 on one side and the source 32 and 34 on the other side. The **floating gates** 28a and 28b are situated in isolation under the **control gates** 36a and 38a, over the oxide isolation region 40a.

Detailed Description Text - DETX (6):
Each **floating gate** 28 forms a tunneling capacitor 57 by its interaction with the channel 58. A tunnel dielectric 56 separates the **floating gate** 28 from the channel 58. Similarly the interpoly dielectric 60 which is part of a coupling capacitor 61, separates the **floating gate** 28 from the

Detailed Description Text - DETX (7):
control gate 36. Finally, the **control gate** 36 is separated by the dielectric 62 from the channel 64.

Detailed Description Text - DETX (8):
The physical relationship of the cells 10, 16, 18 and 20 is illustrated in FIG. 3. The **floating gates** 28 are shown in dashed lines. Similarly, the **control gates** 36 span between the **drain** 38 and a source 32 or 34. **Drain** contacts 42 are located between the **control gates** 36 and bit lines 14, 22, 24 and 26. Bit lines 14, 22, 24 and 26 extend transversely to the **control gates** 36.

Detailed Description Text - DETX (10):
The cells are erased by causing charge to accumulate on the **floating gates** 28 and programming is achieved when charge is removed from the **floating gates**. Thus, initially all of the cells have accumulated charges on their **floating**

gates. All of the cells 10, 16, 18, and 20 are erased together using block erasing.

Detailed Description Text - DETX (11):

Erasing is achieved by high efficiency substrate hot carrier injection. As indicated in FIG. 2, substrate carriers such as the electrons, indicated by the arrows at 66, may be generated by forward biasing a source 32 or 34. That is, the **source** of one cell acts as the injector for the other cell of a **pair** of cells 10, 16, 18, or 20. Thus, the source 32 acts as an injector for the cell 10b being erased in FIG. 2. Similarly, the source 34 acts an injector for the cell 10a when the cell 10a is being erased.

Detailed Description Text - DETX (12):

The source 32 is separated from the cell 10b by the channels 64a and 58 and the **drain** 38. Some of the substrate electrons 66 diffuse through these regions to the channel region 56b underneath the cell 10b. Some electrons are ineffectively taken by the **drain** 38.

Detailed Description Text - DETX (13):

For cells that need to be erased, the channel region 56 may be biased such that a depletion region is formed. When an electron gets to the depletion region, it is accelerated by an electric field, V.sub.CS. The electric field V.sub.CS is the difference between the channel potential (potential of the surface inversion region) and the P-well 44 potential. Some of these electrons gain sufficient energy, in excess of the effective oxide barrier height potential, to be injected onto the **floating gate** 28b.

Detailed Description Text - DETX (14):

For cells that are not to be erased, the channel-to-P-well potential is less then the effective oxide barrier height. In such case, the electrons would not gain sufficient energy to overcome the barrier height and are not injected onto the **floating gate** 28.

Detailed Description Text - DETX (15):

In the case when flash erase is desired, a scheme exists where all the cells inside the same P-well can be erased together. This is achieved by forward-biasing the P-well 44 with respect to the N-well 46. Electrons are injected from the bottom of the P-well 44 as indicated by the arrows 80, and are collected by either the **floating gate or the drain** as shown in FIG. 5.

Detailed Description Text - DETX (16):

The heavily doped N-type source 32, the P-type regions 64a and 56a under the

cell 10a, the region under the **drain** 38 and the cell 10b channel 56b, form a lateral bipolar transistor 68. The emitter (source 32) of the bipolar transistor 68 acts as a charge injector, injecting substrate electrons from the source to the biased depletion region under the **floating gate** 28b. With the source 32 as the emitter and the channels 68a, 56a and the region under the **drain** 38 as the base, the collector is the biased depletion region 56b.

Detailed Description Text - DETX (17):

A compact cell layout is achieved because separate select transistors are unnecessary and the **drain** 38 acts as the **drain** for two adjacent cells in a pair of cells. The **source** of one cell also acts as the efficient injector for the other cell of a **pair**.

Detailed Description Text - DETX (18):

The efficiency of substrate hot electron injection is a function of a number of characteristics. Considering the depletion region 56b, electrons scatter with lattice phonon scattering across the depletion region with a certain electron mean free path. Some of these electrons, without much scattering, gain sufficient energy to overcome the effective barrier height and are injected onto the **floating gate** 28. Some electrons gain less energy than the effective barrier height and are not injected onto the **floating gate** 28. The injection efficiency is a strong function of the **doping** concentrations and the channel-to-P-well potential, V.sub.CS.

Detailed Description Text - DETX (19):

Since the cell 10 is situated in a P-well 44 embedded in an N-well 46, during erasing the **floating gate** 28 is capacitively coupled to a high voltage by raising the potential on the bit lines, which may be biased to a potential from 7 to 14 volts. The voltage that the **floating gate** 28 attains at low **drain** bias is approximately a function of the voltage on the **floating gate when the control gate** 36b and the P-well 44 and **drain** 38 are at ground, plus the coupling ratio times the voltage on the **control gate** 36b. The coupling ratio, to a first order, is approximately equal to the capacitance of the coupling capacitor 61 divided by the sum of the capacitances of the coupling capacitor 61 and the tunneling capacitor 57.

Detailed Description Text - DETX (20):

When the cell 10a is off, the **drain** 38 potential can be forced close to the supply potential V.sub.CC or higher. The channel 56b potential, which is the potential of the surface inversion region of the channel region, is set as follows. When the potential of the **floating gate** 28 (Vfg) is one cell threshold voltage higher than the **drain** 38 potential, the channel potential is

the same as the **drain** potential. On the other hand, when the **floating gate** 28 potential is less than the **drain** 38 potential plus the cell threshold voltage, the channel potential is the difference between the **floating gate** 28 voltage and the cell threshold voltage.

Detailed Description Text - DETX (22):

The potential difference between the channel 56b region and the P-well 44 potential 50 is the voltage across the depletion region. For cells to be erased, the **drain** 38 voltage is raised high, typically close to V.sub.CC or higher. A depletion region underneath the cell being erased is formed with a voltage drop equal to the channel potential minus the P-well potential 50.

Detailed Description Text - DETX (24):

Cell 10 programming is achieved by Fowler-Nordheim tunneling of electrons from the **floating gate** 28 to the channel region 56b and the **drain** 38. During programming, the selected bit line 36b is forced to a high voltage "H" (higher than V.sub.CC) of about 5 volts, for example. The unselected bit lines are maintained at V.sub.SS (external ground). If the N-well and P-well are maintained at V.sub.CC and V.sub.SS respectively, the electric field across the junction between the **drain** 38 and the P-well 44 may be reduced. The reduced field prevents acceleration of hot hole trapping in the gate oxide under the **floating gate** 28. Electrons tunnel to the **drain** 38 (**drain** programming). The tunneling current depends on the voltage from the **floating gate** 28 to the **drain** 38.

Detailed Description Text - DETX (26):

When these potentials are applied to the selected cell 10, a current flows through the cell. This current is then fed to a current sense amplifier (not shown). If the voltage on the **floating gate** 28 is greater than the threshold voltage on the sense transistor 12, a higher current, perhaps greater than 20 microamps, is detected as the conducting state. When the potential of the **floating gate** is less than the threshold voltage, a lower current, for example, less than one microamp flows, and a nonconducting state is detected.

Detailed Description Text - DETX (29):

The voltage across the capacitor 57 is the difference between the **floating gate** 28 potential on the one hand and the **drain** 38 and the P-well 44 potentials. When the difference exceeds 8 to 10 volts, sufficient tunneling current is generated and the **floating gate** 28 can be erased to a negative potential in the time frame of a few milliseconds to a few seconds, depending on the tunneling oxide 56 thickness.

Detailed Description Text - DETX (32):

The starting substrate material is typically P-type (100) silicon, for example having a resistivity in the range of 10-20 ohm-cm. The P-well 44 is embedded in an N-well 46 in the so-called triple well process. The P-well 44 has a typical well depth of, for example, 2 to 4 um with an average **doping** concentration, for example, in the range of 1.times.10.sup.16 to 5.times.10.sup.16 atoms per cubic centimeter.

Detailed Description Text - DETX (33):

The N-well 46 has a typical well depth of, for example, 4-8 um. The **doping** concentration may be from 4.times.10.sup.15 to 1.times.10.sup.16 atoms per cubic centimeter. The triple well is formed by the P-well 44 counterdoping the N-well 46.

Detailed Description Text - DETX (34):

The formation of the elements in the triple well is as follows. An N-well **implant** is done, for example, with phosphorous 31 with a typical dose of 1 to 1.5.times.10.sup.13 atoms per square centimeter and an energy of 160 to 100Kev. The N-well 46 is then counterdoped with a P-well **implant**. Typical dosages for the P-well **implant** could be 1.5 to 2.5.times.10.sup.13 atoms per square centimeter with an energy of 30Kev to 180Kev using a species such as boron 11. The N-well 46 and P-well 28 are then driven, typically 6 to 10 hours at 1125 to 1150.degree. C. This sets the wells to the desired **doping** concentrations and depths.

Detailed Description Text - DETX (35):

After the well formation, standard logic field oxide formation and channel stop formation steps are applied. The field oxide thickness and **implant** doses are adjusted to achieve a field threshold of 7 to 14 volts, which is determined by the level for programming and erasing and by logic process capability. After this formation, a memory cell **implant** may be performed. For example, a B11 **implant** at 30 to 50Kev with a dose of 1.5 to 3.times.10.sup.13 atoms per square centimeter may be done through a sacrificial oxide. The gate oxide 62a and the tunnel oxide 56 are then formed. For example, an 85 to 100 Angstrom dry oxide may be grown across the wafer. A dry oxide is grown, for example, at 900.degree. C. in partial oxygen followed by a 975 to 1050.degree. C. anneal.

Detailed Description Text - DETX (36):

The **floating gate** 28 may then be formed of polysilicon, silicide or metals. If polysilicon is used, it can be 1600 Angstroms thick, and POCL3 doped at 870 to 1000.degree. C. The interpoly dielectric is formed of an oxide-nitride-oxide sandwich (ONO) with the lower oxide being from 60 to 80

Angstroms, the nitride layer having a thickness of from 90 to 180 Angstroms and the upper oxide being from 30 to 40 Angstroms.

Detailed Description Text - DETX (37):

After **floating gate** 28 definition, an N+ **implant** I.sub.1 is implanted into the **drain** side of the device, as shown in FIG. 6. The **implant** I.sub.1 may be subjected to prolonged temperature cycles to form the memory junction. The N+ **implant** can be, for example, a phosphorous **implant** at 60Kev, at a dose of 1 to 3.times.10.sup.14 atoms per square centimeter and may be followed by an arsenic **implant** at 60Kev, 2.5 to 4.5.times.10.sup.15 atoms per square centimeter. It is also possible to form the source and **drain** using lightly doped **drain** (LDD) technology.

Detailed Description Text - DETX (38):

The polysilicon (poly 2) for the **control gate** may then be deposited and silicided if desired. The **control gate** need not be aligned to either edge of the **floating gate**. The **control gate** may be self-aligned to the source, as shown in FIG. 7. The gates are patterned and defined. The **control gate** need not be self-aligned to the **floating gate** on the source or the **drain** sides.

Detailed Description Text - DETX (39):

After **control gate** 36 definition, an N+ source/**drain implant** I.sub.2 may be self-aligned to the **control gate** in conjunction with the formation of sources in the case of memory devices as shown in FIG. 7 and sources and **drains** in the case of logic devices as shown in FIG. 8. Thus, the memory **control gate** 36 forms the gate 88 of the logic devices. At the same time the source region 84 receives the **implant** I.sub.2 with the **drain** covered by the mask 86.

Detailed Description Text - DETX (40):

A resist on resist process may be used to protect interlayer dielectrics such as oxide-nitride-oxide (ONO) layers and the **floating gate from drain implant** contamination. The resist used to define the **floating gate** may be maintained and additional resist may be added to form a composite resist layer 82 to protect logic devices from the memory device **drain implant**. Advantageously, any additional resist used to form the composite resist 82 is spaced back from the **drain** edge to prevent any shadowing during the **drain implant**.

Detailed Description Text - DETX (42):

Referring again to FIG. 3, the flow of electron current from the injector, which in the illustrated embodiment is the source 32, to a **floating gate** 28b is shown. The substrate electrons, indicated by arrows, may flow from the source

32 along the entire width "W" of the cell between adjacent isolation regions 40. In addition, electrons flow from the portions 32a and 32b extending beyond the cell width. Namely, the portions of the source 32 extending to either side of the cell in the width direction also contribute electrons which may be utilized to program the **floating gate** 28. This may significantly increase the available electron current for erasing and thus may expedite erasing.

Detailed Description Text - DETX (43):

This arrangement is possible because the heavily doped N-type sources 32 and 34 run parallel to the **control gates** 36. In other words, the sources 32 and 34 run parallel to the word lines or rows of the array. Because of this geometry, a portion of the source which is greater in length than the width of the cell may be utilized for erasing purposes. Namely, additional electrons may flow from the extensions 32a and 32b between adjacent columns of cells.

Claims Text - CLTX (2):

a **pair of sources and a drain** shaped from one another in the substrate;

Claims Text - CLTX (3):

a **pair of floating gates and a pair** of transistor gates arranged over said substrate between each **source and the drain**; and

Claims Text - CLTX (4):

said sources extending along the width direction of said cell and extending beyond the width of the cells such that said sources can supply charge carriers by substrate hot electron injection to said **floating gates** from a region which is greater than the width of the cells.

Claims Text - CLTX (12):

7. The method of claim 6 including programming said cell by removing charge from a **floating gate**.